CLAIMS

1.   A method for determining a timeout condition in a system having a counter subject to wraparound, comprising:

5   adding a first time value and an offset to produce a sum;

subtracting a second time value from said sum to produce a difference;

masking said difference to produce a masked difference;

10   and,

performing a single compare operation between said masked difference and an expiration value, wherein wraparound ambiguity of said counter is resolved.

15   2.   The method of Claim 1, further comprising;
associating said first time value with a data packet.

3.   The method of Claim 2, further comprising transmitting said data packet when a timeout does not exist.

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4.   The method of Claim 1, further comprising masking two bits of said difference.

5.   The method of Claim 1, further comprising using an 25   arithmetic logic unit (ALU) of a microprocessor to perform said compare operation and said masking.

6.   The method of Claim 1, further including obtaining said first time value and said second time value from a single counter.

5   7.   The method of Claim 1 further including obtaining said first time value from a first counter and obtaining said second time value from a second counter.

8.   The method of Claim 1, further including adding 1
10   to said sum.

9.   A system for determining a timeout condition comprising a first counter with length N coupled to at least one of a plurality of registers, said plurality of registers
15   being coupled to a plurality of logic circuits configured to determine a timeout condition with a single compare operation, wherein wraparound is resolved.

10.   The system of Claim 9, further comprising logic for
20   a masking operation.

11.   The system of Claim 10, further comprising logic for a comparison operation coupled to said logic for a masking operation.
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12.   The system of Claim 9, further comprising at least one register with length of at least N + 2.

13.   The system of Claim 9, further comprising a register for storing an expiration value.

14.   The system of Claim 9, further comprising a register for storing an offset value.

15.   The system of Claim 7, further comprising an adder for performing addition on two inputs coupled to a register with length of at least N + 2.

16.   The system of Claim 7 further comprising a second counter.

17.   A computer readable medium containing executable instructions which, when executed in a processing system, causes the system to perform the steps determining a timeout, comprising:

adding a first time value and an offset to produce a sum;

subtracting a second time value from said sum to produce a difference;

masking said difference to produce a masked difference; and,

performing a first and only compare operation between said masked difference and an expiration value.

18.   The computer readable medium of Claim 17, further comprising instructions for reading a timestamp from a packet header.

5   19.   The computer readable medium of Claim 17, further comprising instructions for loading said first time value from a first counter.

20.   The computer readable medium of Claim 17, further
10   comprising instructions for loading said second time value from a second counter.